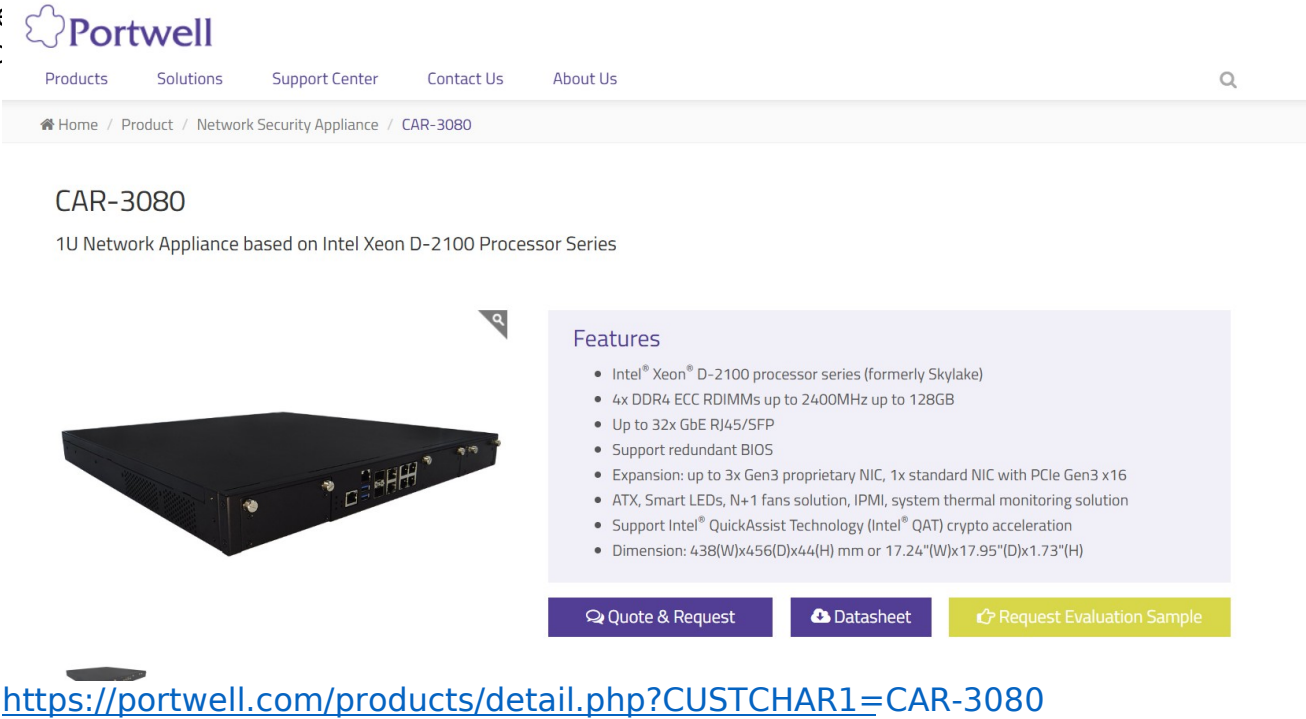


# Exhibit 2

US8234483B2	Portwell CAR-3080 (“Accused Product”)
<p>1. An apparatus implementing a computing and communication chip architecture for integrated circuitry, comprising:</p>	<p>The accused product is an apparatus implementing a computing and communication chip (e.g., PCI Express) architecture for integrated circuitry, comprising:</p> <p>(PCIe) interfaces, Ethernet interface, SATA 3.0, USB 3.0 etc.) architecture for integrated circuitry.</p>  <p><a href="https://portwell.com/products/detail.php?CUSTCHAR1=CAR-3080">https://portwell.com/products/detail.php?CUSTCHAR1=CAR-3080</a></p>



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## CAR-3080

1U Network Appliance based on Intel Xeon D-2100 Processor Series



### Features

- Intel® Xeon® D-2100 processor series (formerly Skylake)
- 4x DDR4 ECC RDIMMs up to 2400MHz up to 128GB
- Up to 32x GbE RJ45/SFP
- Support redundant BIOS
- Expansion: up to 3x Gen3 proprietary NIC, 1x standard NIC with PCIe Gen3 x16
- ATX, Smart LEDs, N+1 fans solution, IPMI, system thermal monitoring solution
- Support Intel® QuickAssist Technology (Intel® QAT) crypto acceleration
- Dimension: 438(W)x456(D)x44(H) mm or 17.24"(W)x17.95"(D)x1.73"(H)

[Quote & Request](#)

[Datasheet](#)

[Request Evaluation Sample](#)

<https://portwell.com/products/detail.php?CUSTCHAR1=CAR-3080>

As shown below, the accused product comprises an Intel Xeon D-2100 processor SOC.

### Introducing the new Intel® Xeon® D-2100 Processor

The new Intel® Xeon® D-2100 processor delivers Intel's most transformative and ground-breaking data center processor architecture in a form factor optimized for flexible, scalable, high-density network, storage and cloud edge solutions. It brings the architectural innovations of the Intel® Xeon® Scalable platform to a system-on-a-chip (SoC) processor for lower-power, high-density solutions, integrating essential network, security and acceleration capabilities. A software-programmable platform featuring robust virtualization support, with low latency, high-bandwidth capabilities through a flexible design, for a variety of solution and service deployments in space and power constrained environments. Design innovation delivers seamless solution scalability from the data center to the network edge.

Designed and manufactured with Intel® Mesh Architecture and using Intel's industry-leading 14nm silicon process technology, the Intel® Xeon® D-2100 processor is the first offering of a line of processors that will address a broad range of lower-power, high-density edge computing needs.

#### Intel® Xeon® D-2100 Processor

Advanced Intelligence for High-Density Edge Solutions

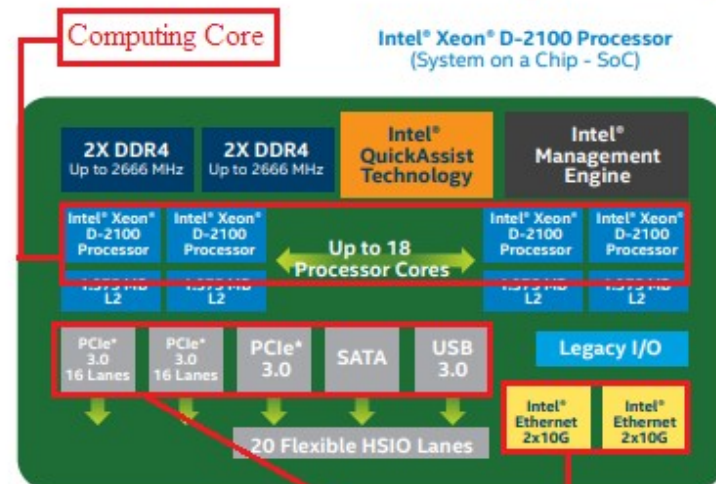


With a range of 4 to 18 cores, up-to 512 GB of addressable memory, this system-on-a-chip (SoC) has an integrated platform controller hub (PCH), integrated high-speed I/O, up-to four integrated 10 Gigabit Intel® Ethernet ports, and a thermal design point (TDP) of 60 watts to 110 watts. It can run the same instruction set as more robust Intel Xeon Scalable processors to provide software consistency and scale from the data center to the edge. It also provides advanced server-class capabilities, including:

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- Built-In Hardware Virtualization using Intel® Virtualization Technology (Intel® VT) to enable dynamic provisioning of services as communication service providers extend network functions virtualization (NFV) to the network edge.
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<https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/xeon-d-2100-product-brief.pdf>

## Intel® Xeon® D-2100 Processor Design Flexibility



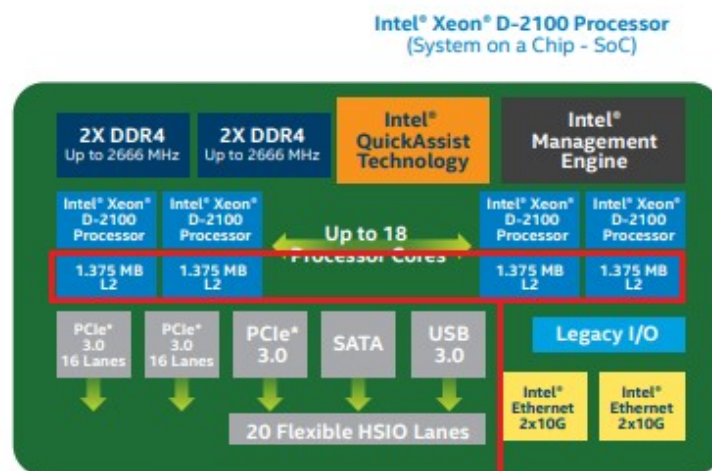
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Maximum Core Count Supported	Up to 18
Maximum Base Frequency Supported	Up to 2.2 GHz
Maximum Intel® Turbo Boost Technology 2.0 Frequency Supported (Single Core)	Up to 3.0 GHz
Processor Cache Memory Support	L2 is 1.375 MB/Core, up-to 24.75 MB featuring rebalanced Intel® Cache hierarchy
Processor Performance Support	Intel® Turbo Boost 2.0 Technology, Intel® Hyper-Threading Technology (Intel® HT), Intel® Speed Shift Technology
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Intel® QuickAssist Technology Support	Available integrated with up to 100 Gbps of crypto, decrypt and encrypt accelerated throughput
Maximum Number of Processor Sockets Supported	One Socket
Thermal Design Point (TDP) Range	Approximately 60 to 110 Watts
Socket Type and Size	Socket FCBGA 45 mm x 52.5 mm
System Memory Support	4 channels of DDR4 2666 MHz 2 DPC RDIMM and LRDIMM with ECC support
Maximum System Memory Supported	Up to 512 GB
PCI Express® Gen 3 Support	Up to 32 lanes
Flexible High-Speed I/O (HSIO)	PCI Express® 3.0 - Up to 20 lanes SATA® 3.0 - Up to 14 lanes USB® 3.0 - Up to 4 ports
Intel® Management Engine (Intel® ME)	Intel® ME 11.11
Intel® Ethernet Support	Available integrated with up to four, 10 GbE adapters with Accelerated Remote Direct Memory Access (RDMA) and native Software Fault Isolation (SFI)

<https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/xeon-d-2100-product-brief.pdf>

at least one memory device; and The accused product comprises a memory device (e.g., L2 Cache or L3 Cache).

## Intel® Xeon® D-2100 Processor Design Flexibility



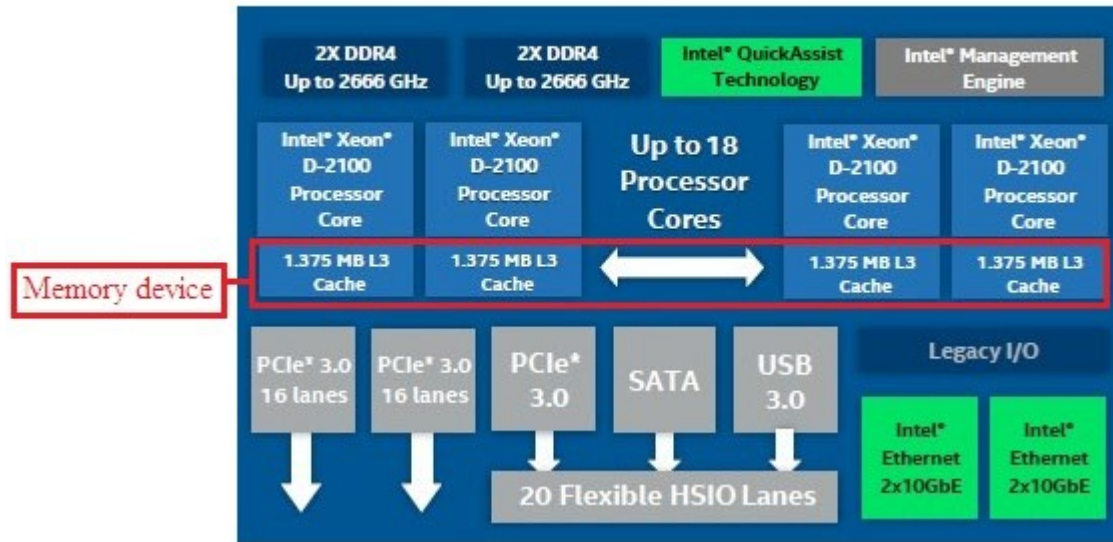
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Below is the block diagram of the Skylake Xeon D:

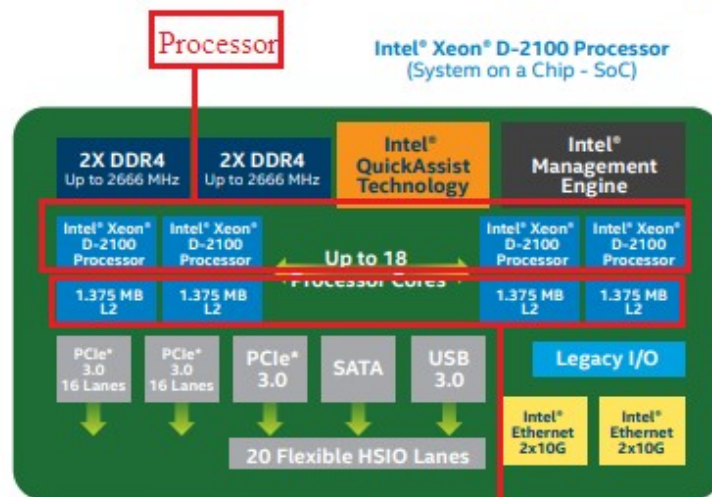


<https://www.nextplatform.com/2018/02/07/intel-sharpens-edge-skylake-xeon-d/>

at least one packet processor uniquely associated with each of the at least one memory device, and

The accused product comprises at least one packet processor (e.g., Intel Xeon D-2100 processor) uniquely associated with each of the memory device (e.g., L2 Cache or L3 Cache).

## Intel® Xeon® D-2100 Processor Design Flexibility

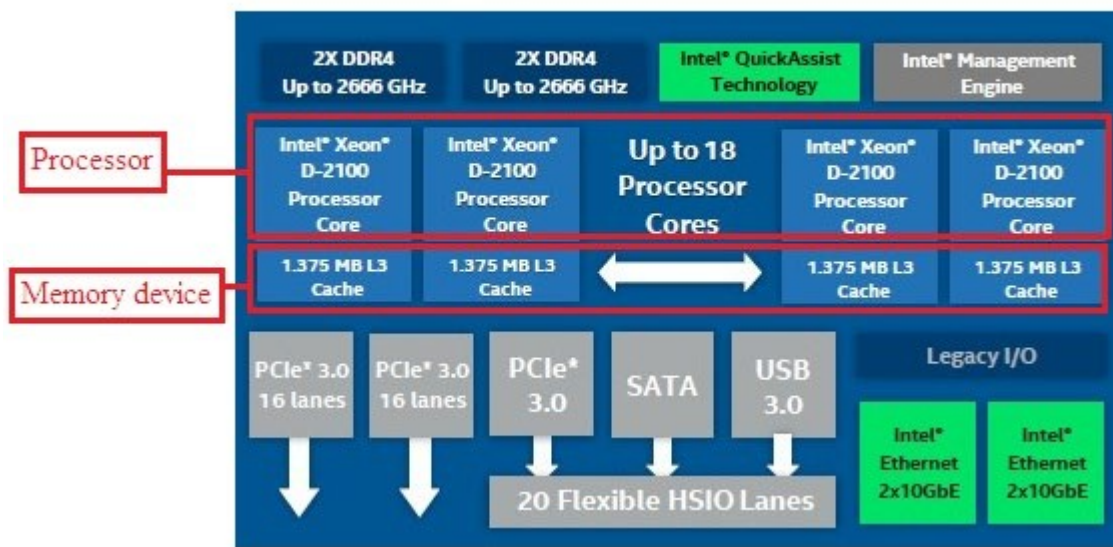


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<https://www.nextplatform.com/2018/02/07/intel-sharpens-edge-skylake-xeon-d/>

the at least one packet processor (e.g., Intel Xeon D-2100 processor) of the accused product is adapted to provide an external device (e.g., a device with which the accused product performs RDMA over Converged Ethernet) read and write access to an external device memory device (e.g., L2 Cache or L3 Cache) via at least one high-speed packet switched serial interface (e.g., Ethernet interface with up to four integrated ports of 10 Gigabit Intel Ethernet), by decapsulating the at least one memory device via at least one high-speed packet switched serial interface, by decapsulating address data and control

information, contained in a packet conforming to a predefined serial protocol format received from the external device, and

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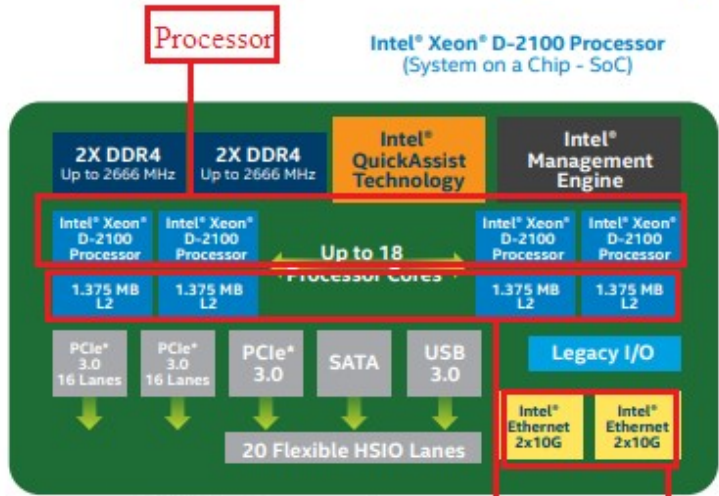


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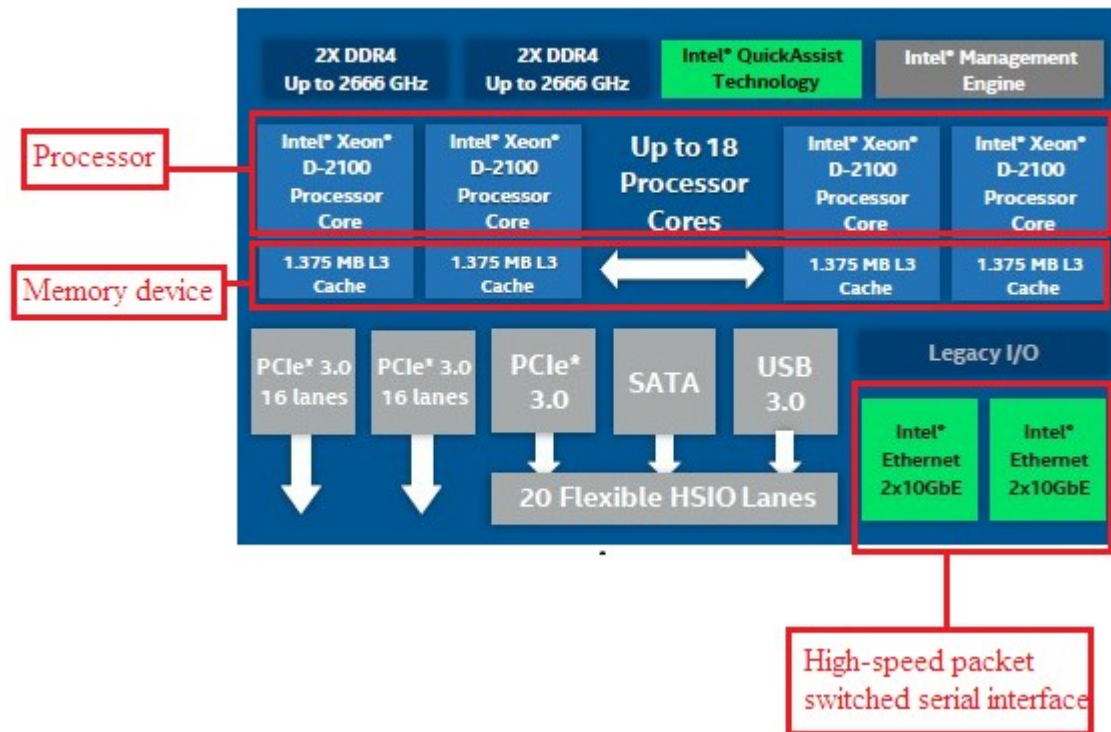
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RDMA over Converged Ethernet (RoCE)

<https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/xeon-d-2100-product-brief.pdf>

Below is the block diagram of the Skylake Xeon D:



<https://www.nextplatform.com/2018/02/07/intel-sharpens-edge-skylake-xeon-d/>

**Intelligent Foundation for Cloud Warm Storage**

**Enhanced capabilities and capacity for cloud warm storage scale-out**

The Intel® Xeon® D-2100 processor provides an intelligent, highly reliable foundation for large-capacity warm storage solutions in cloud environments. Powerful reliability, availability, and serviceability (RAS) features support error-correcting code (ECC) as well as memory and platform-level error management and resilience. Because the processors have built-in hardware virtualization technology and lower-power versions ranging from around 60 to 110 watts, cloud service providers can pack more storage and performance into each rack, improving performance and availability within the same footprint and reducing total cost of ownership. Intel® SSD Data Center Family for NVMe\* delivers fully featured line of solid-state drives to accelerate changes in cloud storage infrastructure and compliment the Intel® Xeon® D-2100 platform.

**Specialty Cloud Services with Web-Tier to Edge**

**Enhancing service scalability for the increasing requirements of content-rich, low-latency, dense data endpoints**

The Intel® Xeon® D-2100 processor provides an intelligent, highly reliable foundation for dense cloud content edge services. Delivers a feature-rich platform to drive a lower total cost of ownership (TCO) for specialty, service-optimized solutions such as web-tier and content delivery cloud edge solutions. Additional cores and threads combined with lower TDP requirements deliver more compute per rack with improved performance/watt. New Intel® Advanced Vector Extensions 512 (Intel® AVX-512) and enhanced Intel® QuickAssist Technology deliver enhanced integrations for faster data transfers, faster encryption and faster cryptography processing, enhancing service scalability for the increasing requirements of content-rich, low-latency, data dense cloud edge services.

<https://www.intel.com/content/www/us/en/products/docs/processors/xeon/d-2100-brief.html>

As shown below, the external device (e.g., a device with which the accused product performs RDMA or Converged Ethernet (RoCE) communication with external network, storage or cloud edge solution) performs read write on the memory device (e.g., L2 Cache or L3 Cache) via at least one high-speed packet switched serial interface (e.g., Ethernet interface with up to four integrated ports of 10 Gigabit Intel Ethernet) through the support of packet processor (e.g., Intel Xeon D-2100 processor).

As shown below, the accused product utilizes RoCE (RDMA protocol over converged Ethernet) to perform read/write operation on the memory device (e.g., L2 Cache or L3 Cache).

## What is RoCE?

- Light-weight RDMA transport over Ethernet
  - Data movement between application memory without CPU involvement
  - RDMA read/write, send-receive and kernel bypass

[http://www.ethernetalliance.org/wp-content/uploads/2011/10/document\\_files\\_RoCE\\_Intro\\_and\\_Update\\_100716](http://www.ethernetalliance.org/wp-content/uploads/2011/10/document_files_RoCE_Intro_and_Update_100716)

## Remote Direct Memory Access

- Direct Memory Access (DMA) allows data to be sent directly from an attached device to the memory on the computer's motherboard.
- The CPU is freed from involvement with the data transfer, thus speeding up overall computer operation
- Remote Direct Memory Access (RDMA): two or more computers communicate directly from the main memory of one system to the main memory of another

UNIVERSITY of HOUSTON

[http://www2.cs.uh.edu/~gabriel/courses/cosc6374\\_f13/ParCo\\_20\\_RDMA.pdf](http://www2.cs.uh.edu/~gabriel/courses/cosc6374_f13/ParCo_20_RDMA.pdf)

2. **Level 2 (L2) cache or Secondary Cache**

There are also L2 caches for larger processors but take longer to access. It is generally part of the CPU, but often a separate chip between the CPU and the RAM.

L2 is a secondary type of cache memory. L2 cache has more capacity than L1. It is located on a computer microprocessor.

The processor searches Instructions in the L1 cache, if required data or instructions not found then it searched into L2 cache. The high-speed system bus interconnecting the cache to the microprocessor.

3. **Level 3 (L3) or Main Memory**

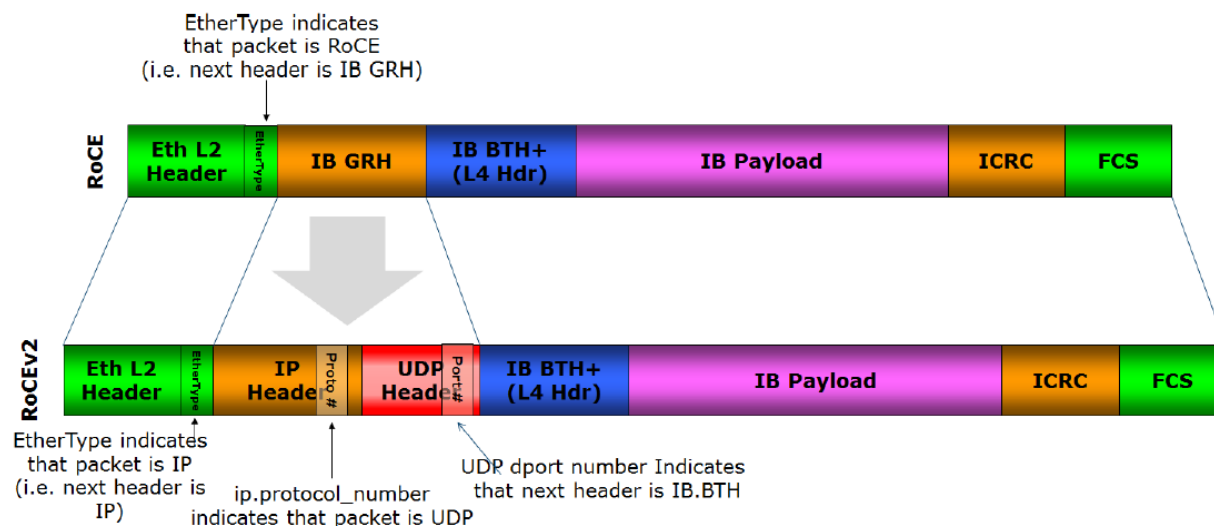
The L3 cache is slower than L1 and L2 but larger. In Multi-core processors, each core may have separate L1 and L2, but all cores share a common L3 cache. L3 cache has double speed than the RAM.

It is a memory on which computer works currently. It is small in size and once power is off data no longer stays in this memory.

As shown below, in RoCEv2 encapsulation of payload is performed to form a RoCEv2 packet.

#### A17.2.4 RoCEv2 (IP ROUTABLE RoCE)

RoCEv2 is a straightforward extension of the RoCE protocol that involves a simple modification of the RoCE packet format. Instead of the GRH, RoCEv2 packets carry an IP header which allows traversal of IP L3 Routers and a UDP header that serves as a stateless encapsulation layer for the RDMA Transport Protocol Packets over IP.



**Figure 3** RoCEv2 and RoCE Frame Format Differences

<https://cw.infinibandta.org/document/dl/7781>

encapsulating data including the decapsulated address and control information into another packet conforming to the

the accused product performs encapsulating data (e.g., RDMA packet) including the decapsulated address and control information into another packet conforming to the said serial protocol format for transmission to an external device, in response to the received packet.

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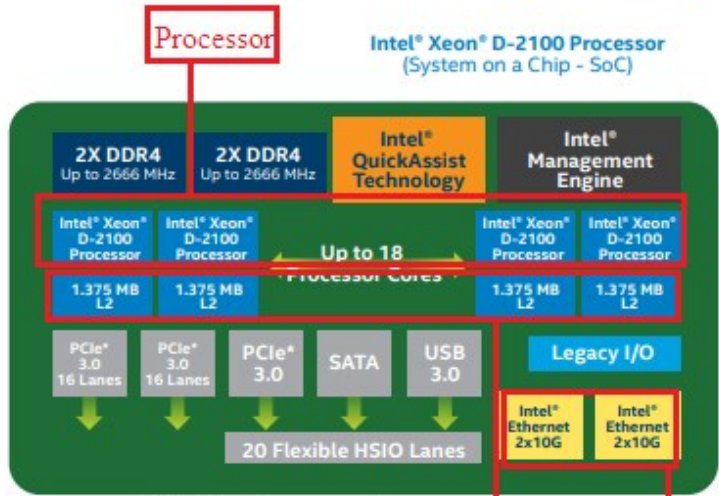


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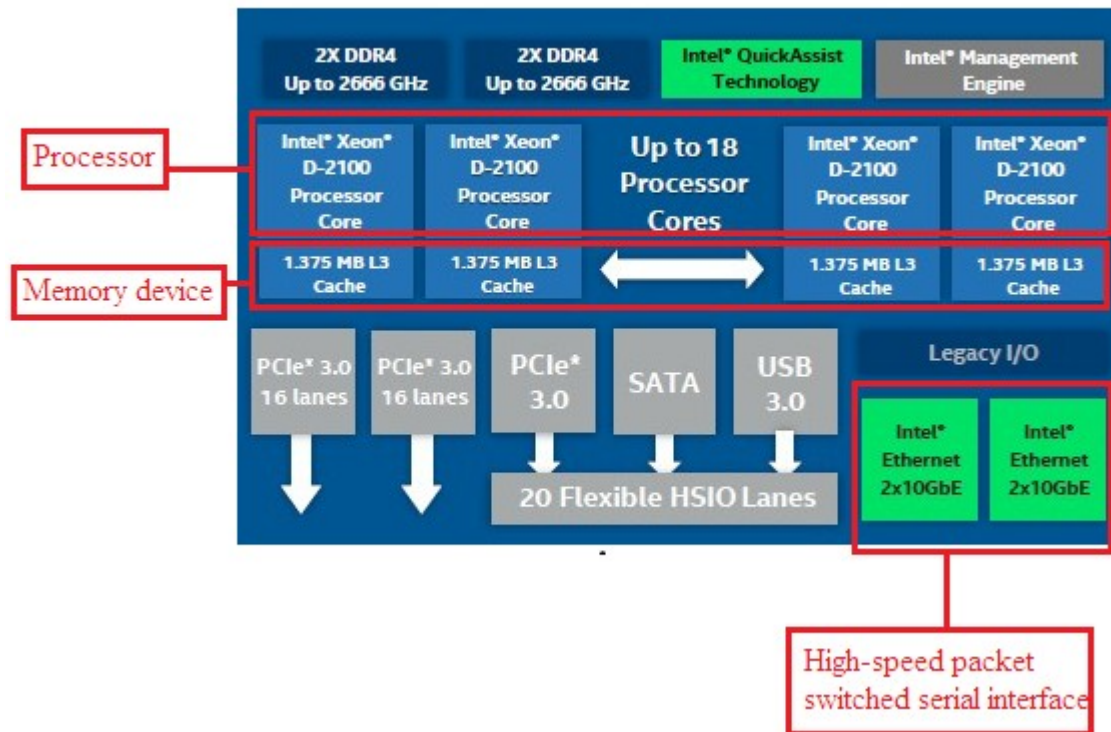
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<https://www.nextplatform.com/2018/02/07/intel-sharpens-edge-skylake-xeon-d/>

**A17.3.1.1.9 SOURCE AND DESTINATION IP ADDRESSES**

**CA17-11:** The Source IP Address of RoCEv2 packets with IPv4 shall be set to the IPv4 address encoded in the Port GID entry referenced by the "port" and "SGID index" components of the Address Vector associated with the packet.

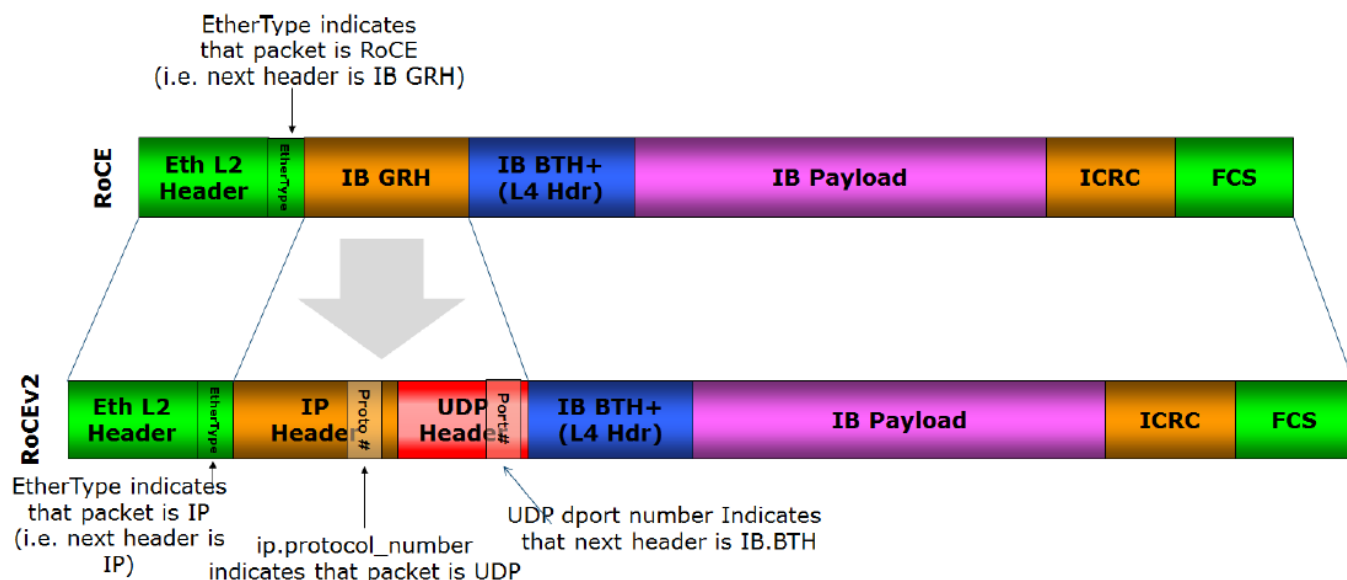
**CA17-12:** The Destination IP Address of RoCEv2 packets with IPv4 shall be set to the IPv4 address encoded in the DGID component of the Address Vector associated with the packet.

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As shown below, in RoCEv2 encapsulation of payload is performed to form a RoCEv2 packet.

#### A17.2.4 RoCEv2 (IP ROUTABLE RoCE)

RoCEv2 is a straightforward extension of the RoCE protocol that involves a simple modification of the RoCE packet format. Instead of the GRH, RoCEv2 packets carry an IP header which allows traversal of IP L3 Routers and a UDP header that serves as a stateless encapsulation layer for the RDMA Transport Protocol Packets over IP.



**Figure 3** RoCEv2 and RoCE Frame Format Differences

<https://cw.infinibandta.org/document/dl/7781>

wherein the at least one memory processor (e.g., Intel Xeon D-2100 processor) are co-located on a semiconductor die package (e.g., on the Intel Xeon D-2100 processor System-on-Chip (SoC) architecture) having at least one external port (e.g., at least one packet integrated ports of 10 Gigabit Intel Ethernet) over which the high-speed packet switched serial interface are co-located on a Ethernet interface with up to four integrated ports of 10 Gigabit Intel Ethernet) is accessible.

semiconductor package having at least one external port over which a high-speed packet switched serial interface is accessible,

### **Introducing the new Intel® Xeon® D-2100 Processor**

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Designed and manufactured with Intel® Mesh Architecture and using Intel's industry-leading 14nm silicon process technology, the Intel® Xeon® D-2100 processor is the first offering of a line of processors that will address a broad range of lower-power, high-density edge computing needs.

**Intel® Xeon® D-2100 Processor**  
Advanced Intelligence for High-Density Edge Solutions

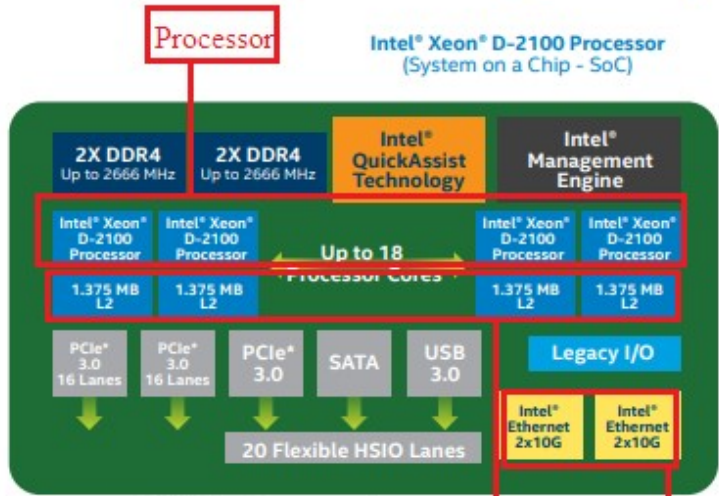


With a range of 4 to 18 cores, up-to 512 GB of addressable memory, this system-on-a-chip (SoC) has an integrated platform controller hub (PCH), integrated high-speed I/O, up-to four integrated 10 Gigabit Intel® Ethernet ports, and a thermal design point (TDP) of 60 watts to 110 watts. It can run the same instruction set as more robust Intel Xeon Scalable processors to provide software consistency and scale from the data center to the edge. It also provides advanced server-class capabilities, including:

- New Intel® Advanced Vector Extensions 512 (Intel® AVX-512) delivers workload-optimized performance and throughput increases for advanced analytics, compute-intensive applications, cryptography and data compression.<sup>†</sup>
- Enhanced Intel® QuickAssist Technology (Intel® QAT), available as an integrated option, delivers chipset-based hardware acceleration, up-to 100 Gbps, for growing cryptography, encryption, and decryption workloads for greater efficiency while delivering enhanced transport and protection across server, storage and network infrastructure.<sup>‡</sup>
- Built-In Hardware Virtualization using Intel® Virtualization Technology (Intel® VT) to enable dynamic provisioning of services as communication service providers extend network functions virtualization (NFV) to the network edge.
- Intel x86 64-bit Software Support for scalable performance and broad application compatibility.
- Enhanced Reliability, Availability, and Serviceability (RAS) features, including support for error-correcting code (ECC) memory and platform-level error management and resilience.
- Intel® Platform Storage Extensions to enable smarter and more cost-effective storage solutions through integrated technologies that accelerate data movement, protect data, and simplify data management.
- Fast Encryption and Decryption Intel® Advanced Encryption Standard New Instructions (Intel® AES-NI) accelerates data

<https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/xeon-d-2100-product-brief.pdf>

Intel® Xeon® D-2100 Processor Design Flexibility



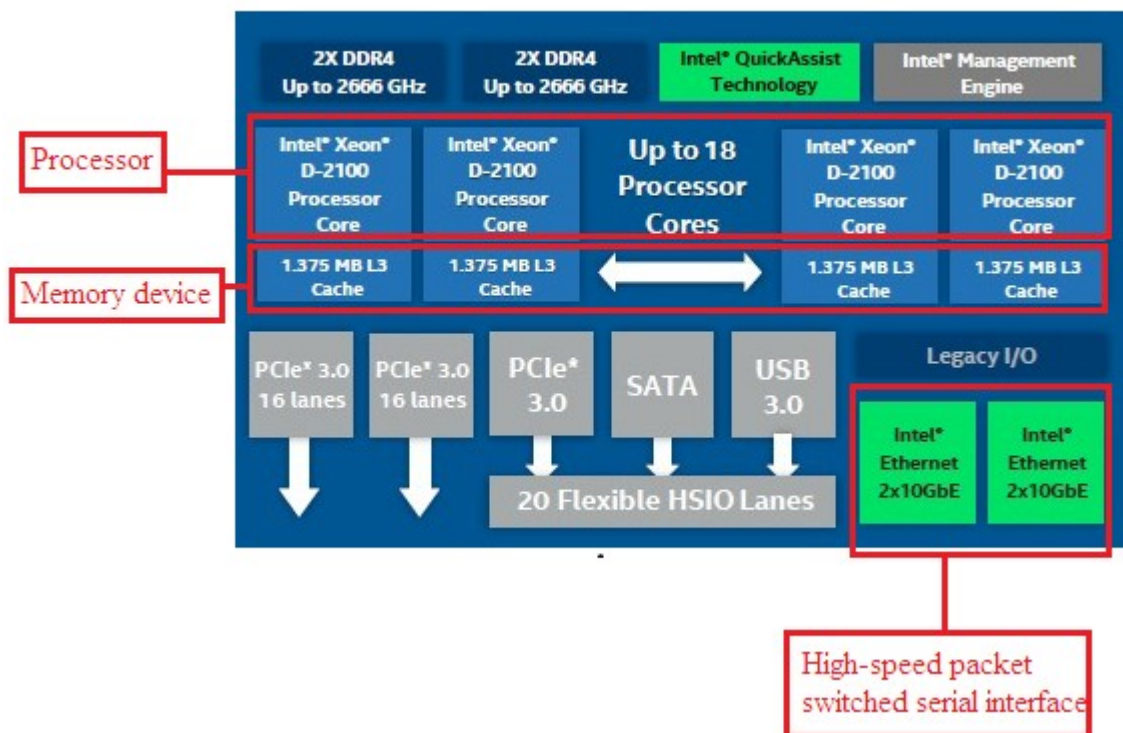
Diagrams are provided for illustration purposes only. Diagrams (above) and table (right) are not a comprehensive list of product features or capabilities. Product details and features are subject to change without notice.

Processor Manufacturing Process	Intel's optimized 14nm process technology featuring Intel® Mesh Architecture
Maximum Core Count Supported	Up to 18
Maximum Base Frequency Supported	Up to 2.2 GHz
Maximum Intel® Turbo Boost Technology 2.0 Frequency Supported (Single Core)	Up to 3.0 GHz
Processor Cache Memory Support	L2 is 1.375 MB/Core, up-to 24.75 MB featuring rebalanced Intel® Cache hierarchy
Processor Performance Support	Intel® Turbo Boost 2.0 Technology, Intel® Hyper-Threading Technology (Intel® HT), Intel® Speed Shift Technology
Intel® Advanced Vector Extension 512 (Intel® AVX-512) Support	Intel® AVX-512 with up to 1 FMA support
Intel® QuickAssist Technology Support	Available integrated with up to 100 Gbps of crypto, decrypt and encrypt accelerated throughput
Maximum Number of Processor Sockets Supported	One Socket
Thermal Design Point (TDP) Range	Approximately 60 to 110 Watts
Socket Type and Size	Socket FCBGA 45 mm x 52.5 mm
System Memory Support	4 channels of DDR4 2666 MHz 2 DPC RDIMM and LRDIMM with ECC support
Maximum System Memory Supported	Up to 512 GB
PCI Express® Gen 3 Support	Up to 32 lanes
Flexible High-Speed I/O (HSIO)	PCI Express® 3.0 - Up to 20 lanes SATA® 3.0 - Up to 14 lanes USB® 3.0 - Up to 4 ports
Intel® Management Engine (Intel® ME)	Intel® ME 11.11
Intel® Ethernet Support	Available integrated with up to four, 10 GbE adapters with Accelerated Remote Direct Memory Access (RDMA) and native Software Fault Isolation (SFI)

RDMA over Converged Ethernet (RoCE)

<https://www.intel.com/content/dam/www/public/us/en/documents/product-briefs/xeon-d-2100-product-brief.pdf>

Below is the block diagram of the Skylake Xeon D:



<https://www.nextplatform.com/2018/02/07/intel-sharpens-edge-skylake-xeon-d/>

such that the high-speed packet switched serial device (e.g., a device with which the accused product performs RDMA over Converged Ethernet) receives the said packet (e.g., RoCE packet transmitted to external device) to the said external device. The high-speed packet switched serial interface (e.g., Ethernet interface with up to four integrated ports) of the accused product receives the said packet (e.g., RoCE packet received from external device) and transmits the said packet (e.g., RoCE packet transmitted to external device) to the said external device.

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Advanced Intelligence for High-Density Edge Solutions



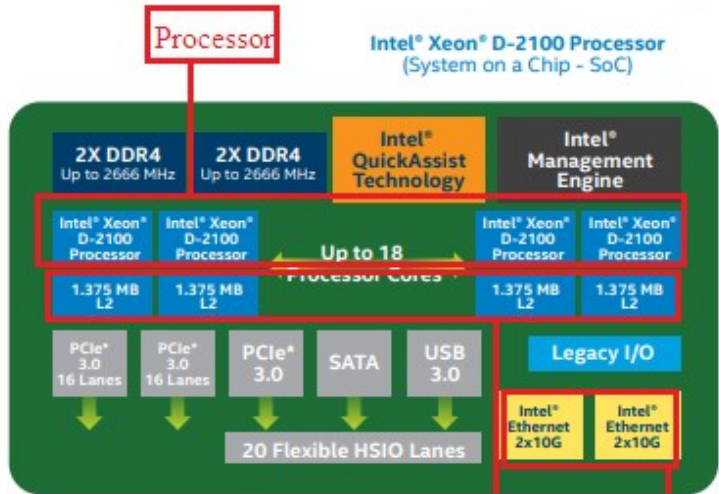
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As shown below, the accused product performs RoCE.

**Intel® Xeon® D-2100 Processor Design Flexibility**



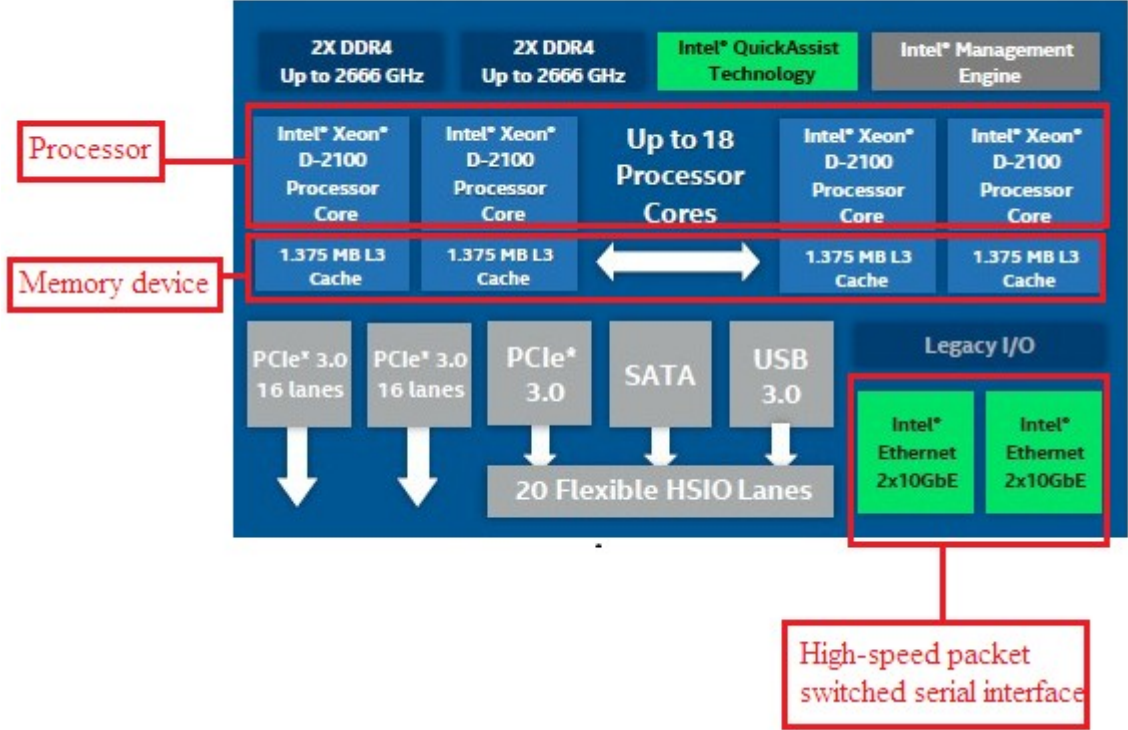
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#### **Intelligent Foundation for Cloud Warm Storage**

##### **Enhanced capabilities and capacity for cloud warm storage scale-out**

The Intel® Xeon® D-2100 processor provides an intelligent, highly reliable foundation for large-capacity warm storage solutions in cloud environments. Powerful reliability, availability, and serviceability (RAS) features support error-correcting code (ECC) as well as memory and platform-level error management and resilience. Because the processors have built-in hardware virtualization technology and lower-power versions ranging from around 60 to 110 watts, cloud service providers can pack more storage and performance into each rack, improving performance and availability within the same footprint and reducing total cost of ownership. Intel® SSD Data Center Family for NVMe\* delivers fully featured line of solid-state drives to accelerate changes in cloud storage infrastructure and compliment the Intel® Xeon® D-2100 platform.

#### **Specialty Cloud Services with Web-Tier to Edge**

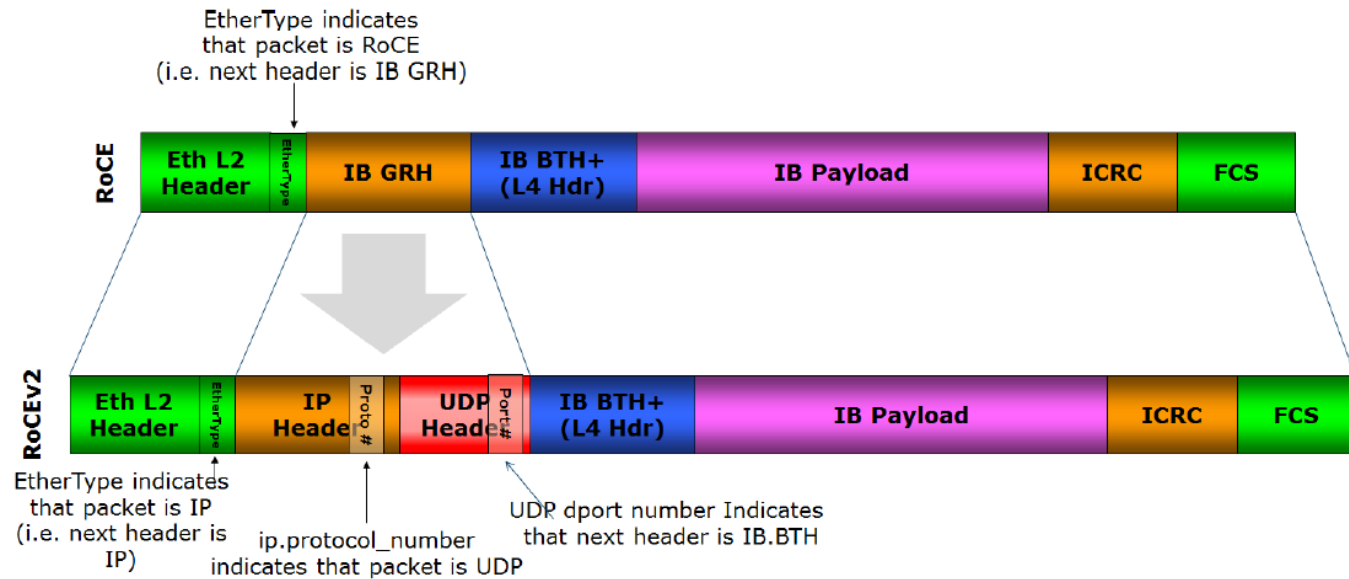
##### **Enhancing service scalability for the increasing requirements of content-rich, low-latency, dense data endpoints**

The Intel® Xeon® D-2100 processor provides an intelligent, highly reliable foundation for dense cloud content edge services. Delivers a feature-rich platform to drive a lower total cost of ownership (TCO) for specialty, service-optimized solutions such as web-tier and content delivery cloud edge solutions. Additional cores and threads combined with lower TDP requirements deliver more compute per rack with improved performance/watt. New Intel® Advanced Vector Extensions 512 (Intel® AVX-512) and enhanced Intel® QuickAssist Technology deliver enhanced integrations for faster data transfers, faster encryption and faster cryptography processing, enhancing service scalability for the increasing requirements of content-rich, low-latency, data dense cloud edge services.

<https://www.intel.com/content/www/us/en/products/docs/processors/xeon/d-2100-brief.html>

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